USING NETWORK WIRING TO SUPPLY POWER TO NETWORKED

DEVICES MAKES INSTALLING THE DEVICES MUCH EASIER. WHEREAS

POE (POWER-OVER-ETHERNET) DESIGNS AREN'T ROCKET SCIENCE,

DESIGNERS STILL HAVE TO KNOW WHAT THEY'RE DOING.

Don't overlook cable and connector imbalances in POE applications

ONE OF THE GREAT SUCCESS STORIES of the information age has been the advent of LANs. By interconnecting PCs and their peripherals into a common LAN, you can share all the information and work of each. With implementation costs steadily decreasing, LAN connections now enable you to use devices that you once couldn't economically justify. IP (Internet Protocol) telephony, Web cameras, wireless access points, home automation, and building management represent just a few examples.

In some markets, the costs associated with providing power to the connected devices have presented barriers to LAN interconnection. In an effort to control these costs, the IEEE 802.3 working group is developing a POE (power-over-Ethernet) standard, IEEE 802.3af, that will allow the data link to provide each connected device with as much as 12.95W of unregulated dc power.

The PSE (power-sourcing equipment) injects a phantom current into a transformer's center tap, where it divides and passes through one of two pairs of balanced transmission lines (**Figure 1**). At the far end, the two currents pass into a transformer in which they recombine to form the power source for the PD (powered device). The device's return path uses the other pair of balanced transmission lines. The proposed standard sets at 350 mA total (or 175 mA per path) the maximum current that the device can continuously draw.

One drawback that you should always consider in implementing this scheme is the cabling's resistive imbalance. A typical cabling channel can contain as many as five interconnects and 100m of wire (**Figure 2**). In the proposed standard, the resistance balance between the channel's two paths, which is specified not to exceed 3% of the sum of the resistances in the two paths, is computed as follows:

$$\left(\frac{(R_{MAX} - R_{MIN})}{(R_{MAX} + R_{MIN})} \right) \bullet 100 = PERCENT, \qquad (1)$$

where R_{MAX} is the path with the higher resistance, and R_{MIN} is the path with the lower resistance.

At the maximum current, this imbalance equates to a 10.5-mA bias on the transformer's core. Under all tolerance and temperature conditions, transformers for 100BaseTX applications have a minimum inductance of 350 μH with 8 mA or less of dc bias. A transformer that can tolerate only this amount of bias reduces the maximum current the power-sourcing equipment can deliver before the transformer saturates to:

$$350 \text{ mA} \bullet \left(\frac{8 \text{ mA}}{10.5 \text{ mA}} \right) = 267 \text{ mA}. \qquad (2)$$

Consider the case in which only a 5m patch cable separates the power-sourcing equipment and the powered device. These conditions, which don't comply with the proposed standard, can cause the current imbalance to exceed 42 mA. You can verify this fact by setting R_B in **Equation 3** to zero and solving for I_{IMBAL}.

Figure 1
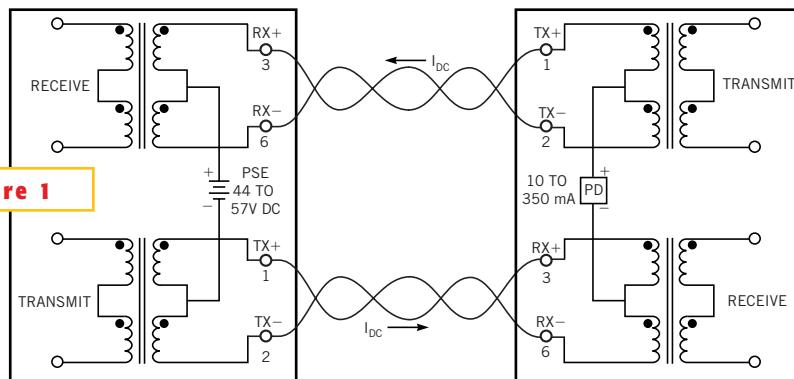
The PSE injects a phantom current into a transformer's center tap, where it divides and passes through one of two pairs of balanced transmission lines. At the far end, the two currents pass into a transformer in which they recombine to form the power source for the PD.

To restore the current capability to 350 mA, you must employ a ballast circuit. **Figure 3** details a method for resolving cable and connector imbalances by using two resistors. Note that each end of the transmitting and the receiving channels requires these ballast resistors. Adding the capacitor in parallel with the resistors helps to minimize the signal loss that results from the ballast resistors. You should select the capacitor to present a low impedance at the lowest signal frequency. Although the capacitor's value depends on the implementation, selecting 0.22 μF results in less than 0.5 dB of loss at 100 kHz.

Table 1 details the resistance of different cable sizes over minimum and maximum temperature ranges. Subsequent calculations use these resistance values to resolve connector imbalances and voltage drops.

For calculating the ballast resistors, the typical maximum configuration uses five connectors. In each connection point, one contact measures 0Ω, whereas the other contact measures 0.02Ω—the maximum resistance that IEC 512-2 allows (**Reference 1**). Furthermore, the model uses a 5m length of 22 AWG cable, because longer cable reduces the effect of the connectors' contribution to the imbalance. The equations describing this interaction are:

$$\left(\frac{I_{OUT} + I_{IMBAL}}{2} \bullet \left(\frac{R_C}{1.03} + \frac{R_B}{1.01} \right) \right) =$$
$$\left(\begin{array}{c} \frac{I_{OUT} - I_{IMBAL}}{2} \bullet (R_C \bullet 1.03 + R_B \bullet \\ 1.01 + R_{CONNECT}) \end{array} \right), \quad (3)$$

where I_{OUT} (the maximum current from the PSE)=350 mA, I_{IMBAL} (the current difference between the two pairs)=58 mA, R_C (5m of 22 AWG cable)=0.24Ω, R_B (the ballast resistance)=6.6Ω, and R_{CONN} (the total contact resistance for five connectors)=0.1Ω.

Under these conditions, the worst-case current imbalance is 6.25 mA. Using 3.3Ω ballast resistors increases the total voltage drop associated with the cabling by:

$$\left(175 + \frac{6.25}{2} \right) mA \bullet (4 \bullet 3.3\Omega) = 2.35V. \quad (4)$$

Figure 2

CHANNEL

PERMANENT LINK

HUB · C · C · C · C · C · NIC

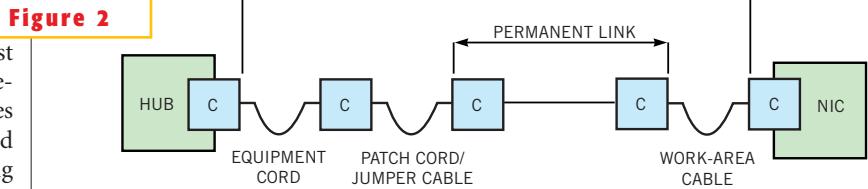EQUIPMENT CORD · PATCH CORD/ JUMPER CABLE · WORK-AREA CABLE

NOTES: C=CONNECTION.
NIC=NETWORK-INTERFACE CARD.

In implementing POE, you should always consider the cabling's resistive imbalance. A typical cabling channel can contain as many as five interconnects and 100m of wire.
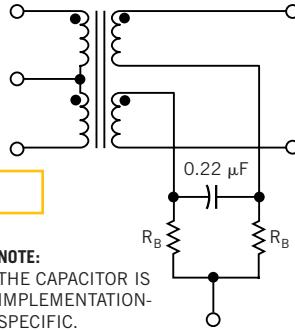

0.22 μF

R_B R_B

Figure 3

NOTE:
THE CAPACITOR IS IMPLEMENTATION-SPECIFIC.

To restore the current capability to 350 mA, you need a ballast circuit. This method for resolving cable and connector imbalances uses two resistors at each end of both the transmitting and the receiving channels.

The proposed standard requires the equipment to supply a minimum voltage greater than 44V and the powered device to present a maximum voltage no larger than 36V. At the maximum current, this 8V margin permits as much as 45.7Ω of resistance per conductor path between the power-sourcing equipment and the device. Even under worst-case temperature and tolerance conditions, using 3.3Ω ballast resistors in series with 100m of 26 AWG cable still provides a margin of:

$$8V - (175 \text{ mA} \bullet$$
$$\left(30.86\Omega + \frac{0.1\Omega}{2} + 4 \bullet 3.3\Omega \right) = 0.28V. \quad (5)$$

The ballast resistors dissipate worst-case power during an overcurrent condition, which the proposed standard sets at 450 mA. In this case, the wattage rating of the ballast resistors is:

$$\left(\frac{450 \text{ mA}}{2} \right)^2 \bullet 3.3\Omega = 0.17W. \quad (6)$$

Therefore, a resistor having a 0.25W rating suffices.

With this latest IEEE-proposed standard, LAN devices requiring modest amounts of power now have the option of receiving it from a central hub. However, when employing this feature, you should consider adding ballast resistors to eliminate the possibility of saturating the isolation transformers.

An alternative to implementing ballast resistors is to design a custom magnetic module that can accommodate the added offset current. The downside of this approach is added cost and module size, due mainly to the design's requiring a larger magnetic structure. Furthermore, it is economically unrealistic to design a transformer that can tolerate the 42 mA possible when minimal distances separate the power-sourcing equipment from the powered device.

Of course, you can elect to do nothing, in which case the transformer may saturate, and the burden of signal restoration will fall on the baseline-wander-correction circuits in the physical-layer chip. Unfortunately, some legacy LAN chips lack such circuits.□

REFERENCE
1. IEC 512-2, Electromechanical Components for Electronic Equipment; Basic Testing Procedures and Measuring Methods; Part 2: General Examination, Electrical Continuity and Contact Resistance Tests, Insulation Tests, and Voltage Stress Tests.

AUTHOR'S BIOGRAPHY
Hank Hinrichs has worked as a design engineer at Pulse for more than 30 years. During that time, he has been involved in the design of numerous dc/dc converters, filters, and other magnetic modules for both the LAN and the telecommunications industries.

TABLE 1—CABLE RESISTANCES

AWG	Minimum at 0℃ (Ω/100m)	Maximum at 0℃ (Ω/100m)	Nominal (Ω/100m)	Minimum at 500℃ (Ω/100m)	Maximum at 500℃ (Ω/100m)
26	12.18	12.79	13.47	14.7	15.43
24	7.65	8.03	8.42	9.14	9.6
22	4.81	5.05	5.31	5.79	6.08